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APPLICATION NO. 1177382, 887	FILING DATE 07/15/99	FIRST NAMED INVENTOR EDWARDS	ATTORNEY DOCKET NO.
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WM02/0925

EXAMINER
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CHUNG, D

ART UNIT	PAPER NUMBER
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2672

*11*

DATE MAILED:

09/25/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

*SM*

# Office Action Summary

Application No.

09/353,887

Applicant(s)

EDWARDS, STEPHEN W.

Examiner

Daniel J Chung

Art Unit

2672

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 12 July 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-38 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-38 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 10. 6) ☐ Other:

## **DETAILED ACTION**

Claims 1-38 are presented for examination. This office action is in response to the amendment filed on 7-12-2001.

### ***Information Disclosure Statement***

Receipt is acknowledged of Applicant's Information Disclosure Statement of 9-10-2001, which has been placed in the application file and considered by the Examiner.

### ***Specification***

Please review the application and correct all informalities.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1,2,5-7,9-13 and 15-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaneko (5,764,237) in view of Tanaka et al.

Regarding claim 1, Kaneko discloses that the claimed feature of a graphics accelerator for processing a graphical image, (See Abstract, Fig 1, Fig 2, col 2 line 35-col 4 line 39, col 5 line 8-32, col 6 line 6-56, col 11 line 27-55, col 11 line 57+) the graphics accelerator comprising:

A texture buffer (texture memory; 5) for storing texture maps and data relating to the texture maps stored in the texture buffer (5) (See Abstract, Fig 1, col 2 line 35-col 4 line 39, col 5 line 8-32)

A texture processor (texture mapping unit; 1) that performs texturing operations on the graphical image (See Abstract, Fig 1, col 2 line 35-col 4 line 39, col 5 line 8-32)

The texture processor (1) including a fetching engine (selector; 15) that retrieves texture packets (texture address data, which generated by texture address generator; 13), each texture packet being stored in the texture buffer (5) and being associated with a texture map, each texture packet including data relating to the location (identified by texture address) of its associated texture map in the texture buffer (5) (See Abstract, Fig 1, Fig 2, col 2 line 35-col 4 line 39, col 5 line 8-32, col 6 line 6-56, col 11 line 27-55, col 11 line 57+)

Kaneko does not specifically disclose that "texture buffer", as claimed by Applicant. However, a texture buffer is an obvious embodiment of the notoriously well-known texture memory. According to the on-line computer dictionary, buffer is defined as "a region of memory reserved for use as an intermediate repository in which data is temporarily held while waiting to be transferred between two locations, as between an

application's data area and an input/output device". From its definition of "buffer", it is reasonable to interpret the texture buffer as a part/same of texture memory. Therefore, it would have been obvious to one skilled in the art to "texture buffer" into the teaching of Kaneko.

Also, Kaneko does not explicitly disclose that a texture packets identifying the location of a texture map. [Although Examiner still can consider the limitation "texture address data" in the teaching of Kaneko as "texture packets" in the broadly claimed invention] However, Tanaka et al discloses that the packet data, which represents the storage location of a texture data/map. (See col 2 line 55-62, col 8 line 26-34) The motivation would have been to provide enhanced image data by converting the existing file format [ex. texture data, texture address data] into the new improved format [e.g. texture packet], as mentioned in the teaching of Tanaka et al. (See col 2 line 55-col 3 line 43) Therefore, it would have been obvious to one skilled in the art to incorporate the teaching of Tanaka et al into the teaching of Kaneko.

Regarding claim 2, Kaneko discloses that each texture packet is associated with a texture map that is different than the texture maps associated with any other texture packet in the texture buffer. (See Abstract, Fig 1, Fig 2, col 2 line 35-col 4 line 39, col 5 line 8-32, col 6 line 6-56, col 11 line 27-55, col 11 line 57+)

Regarding claim 5, Kaneko discloses that an input for receiving a texture message indicating that a texture map is to be utilized by the texture processor, the fetching engine responsively retrieving selected texture packets from the texture buffer in response to receipt of the texture message. (See Abstract, Fig 1, Fig 2, col 2 line 35-col 4 line 39, col 5 line 8-32, col 6 line 6-56, col 11 line 27-55, col 11 line 57+)

Regarding claim 6, Kaneko discloses that the texture processor includes a parsing engine for parsing a fetched texture packet and determining information relating to the texture map associated with the fetched texture packet. (See Abstract, Fig 1, Fig 2, col 2 line 35-col 4 line 39, col 5 line 8-32, col 6 line 6-56, col 11 line 27-55, col 11 line 57+)

Regarding claim 7, Kaneko discloses that the information relates to the location in the texture buffer of the texture map associated with the fetched texture packet. (See Abstract, Fig 1, Fig 2, col 2 line 35-col 4 line 39, col 5 line 8-32, col 6 line 6-56, col 11 line 27-55, col 11 line 57+)

Regarding claim 9, Kaneko discloses that the claimed feature of a method of applying texture to a graphical image, (See Abstract, Fig 1, Fig 2, col 2 line 35-col 4 line 39, col 5 line 8-32, col 6 line 6-56, col 11 line 27-55, col 11 line 57+) the method comprising:

Locating a texture packet (texture address data) identifying the location of a texture map in a memory device (texture memory; 5) (See Abstract, Fig 1, Fig 2, col 2 line 35-col 4 line 39, col 5 line 8-32)

Parsing the texture packet to determine the location of the texture map (See Abstract, Fig 1, Fig 2, col 2 line 35-col 4 line 39, col 5 line 8-32)

Retrieving, based upon the determined location, the texture map from the memory device (See Abstract, Fig 1, Fig 2, col 2 line 35-col 4 line 39, col 5 line 8-32)

Applying the texture map to the graphical image. (See Abstract, Fig 1, Fig 2, col 2 line 35-col 4 line 39, col 5 line 8-32)

Regarding claim 10, Kaneko discloses that the texture packet is located by accessing a record identifying the location of the texture packet. (See Abstract, Fig 1, Fig 2, col 2 line 35-col 4 line 39, col 5 line 8-32, col 6 line 6-56, col 11 line 27-55, col 11 line 57+)

Regarding claim 11, Kaneko discloses that the memory device is texture memory. (See Abstract, Fig 1, Fig 2, col 2 line 35-col 4 line 39, col 5 line 8-32, col 6 line 6-56, col 11 line 27-55, col 11 line 57+)

Regarding claim 12, Kaneko discloses that the texture packet is stored in the memory device. (See Abstract, Fig 1, Fig 2, col 2 line 35-col 4 line 39, col 5 line 8-32, col 6 line 6-56, col 11 line 27-55, col 11 line 57+)

Regarding claim 13, Kaneko discloses that reconstructing the texture map after it is retrieved from the memory device. (See Abstract, Fig 1, Fig 2, col 2 line 35-col 4 line 39, col 5 line 8-32, col 6 line 6-56, col 11 line 27-55, col 11 line 57+)

Regarding claims 15-19, claims 15-19 are similar in scope to the claims 9-13, and thus the rejections to claims 9-13 hereinabove are also applicable to claims 15-19.

Claims 3,4,8,14,20-25 and 35-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaneko in view of Tanaka et al as applied to claim 1 above, and further in view of Priem et al (6,191,794).

Regarding claim 3, Kaneko discloses that each texture packet includes data relating to the dimensional type of its associated texture map. (See Abstract, Fig 1, Fig 2, col 2 line 35-col 4 line 39, col 5 line 8-32, col 6 line 6-56, col 11 line 27-55, col 11 line 57+)

Kaneko does not specifically disclose that texture data is relating to the dimensional type of its texture map. However, Priem et al discloses that the step of determine the change of dimensions in the texture map with respect to the change in the dimensions of pixel in the process of texture mapping. (See col 8 line 5-9, col 8 line



20-28) The motivation would have been to provide for much faster manipulation of the texture coordinates to obtain texture values and thereby eliminates the need for complicated and expensive circuitry in the graphics accelerator, as mentioned in the teaching of Priem et al. (See col 8 line 20-26) Therefore, it would have been obvious to one skilled in the art to incorporate the teaching of Priem et al into the teaching of Kaneko. Furthermore, the step of sorting the texture data with respect to the type of its dimension was well-know art to one having the ordinary skilled in the art, in order to operate texture mapping processing efficiently. The ordinary skilled in the art would know that the three-dimensional texture mapping process will require large capacity processor and much more time to process comparing to one-dimensional texture mapping process, since 3-D texture mapping have more variable to calculate. Therefore, it would have been obvious to one skilled in the art to separate the texture data by its dimensional type.

Regarding claim 4, refer to the discussion for the claim 3 hereinabove, Kaneko discloses that the dimensional type of each texture map is one of a one-dimensional texture map, a two-dimensional texture map, and a three-dimensional texture map. (See Abstract, Fig 1, Fig 2, col 2 line 35-col 4 line 39, col 5 line 8-32, col 6 line 6-56, col 11 line 27-55, col 11 line 57+)

Regarding claim 8, refer to the discussion for the claim 3 hereinabove, Kaneko discloses that the information relates to the number of dimensions of the texture map associated with the fetched texture packet. (See Abstract, Fig 1, Fig 2, col 2 line 35-col 4 line 39, col 5 line 8-32, col 6 line 6-56, col 11 line 27-55, col 11 line 57+)

Regarding claim 14, refer to the discussion for the claim 3 hereinabove, Kaneko discloses that the texture packet includes data relating to the dimensional type of the texture map, the texture map being reconstructed by parsing the texture packet to determine the dimensional type of the texture map, the texture map being reconstructed based upon the determined dimensional type of the texture map. (See Abstract, Fig 1, Fig 2, col 2 line 35-col 4 line 39, col 5 line 8-32, col 6 line 6-56, col 11 line 27-55, col 11 line 57+)

Regarding claim 20, claim 20 is similar in scope to the claim 14, and thus the rejection to claim 14 hereinabove is also applicable to claim 20.

Regarding claim 21, claim 21 is similar in scope to the claim 1, and thus the rejection to claim 1 hereinabove is also applicable to claim 21.

In addition, Kaneko fails to teach that texture data is relating to the dimensional type of its texture map. However, Priem et al discloses that the step of determine the change of dimensions in the texture map with respect to the change in the dimensions of pixel in the process of texture mapping. (See col 8 line 5-9, col 8 line 20-28) The

motivation would have been to provide for much faster manipulation of the texture coordinates to obtain texture values and thereby eliminates the need for complicated and expensive circuitry in the graphics accelerator, as mentioned in the teaching of Priem et al. (See col 8 line 20-26) Therefore, it would have been obvious to one skilled in the art to incorporate the teaching of Priem et al into the teaching of Kaneko. Furthermore, the step of sorting the texture data with respect to the type of its dimension was well-know art to one having the ordinary skilled in the art, in order to operate texture mapping processing efficiently. The ordinary skilled in the art would know that the three-dimensional texture mapping process will require large capacity processor and much more time to process comparing to one-dimensional texture mapping process, since 3-D texture mapping have more variable to calculate. Therefore, it would have been obvious to one skilled in the art to separate the texture data by its dimensional type.

Regarding claims 22-23, claims 22-23 are similar in scope to the claims 1-2, and thus the rejections to claims 1-2 hereinabove are also applicable to claims 22-23.

Regarding claims 24-25, claims 24-25 are similar in scope to the claims 5-6, and thus the rejections to claims 5-6 hereinabove are also applicable to claims 24-25.

Regarding claim 35, refer to the discussion for the claim 3 hereinabove, Kaneko discloses that the claimed feature of a data structure for storing data relating to a texture

map, the texture map having an associated dimension and being stored at a given location in a memory device, the apparatus comprising:

A location field identifying the given location in the memory device (See Abstract, Fig 1, Fig 2, col 2 line 35-col 4 line 39, col 5 line 8-32, col 6 line 6-56, col 11 line 27-55, col 11 line 57+)

A dimension field identifying the dimension of the texture map (See Abstract, Fig 1, Fig 2, col 2 line 35-col 4 line 39, col 5 line 8-32, col 6 line 6-56, col 11 line 27-55, col 11 line 57+)

Regarding claim 36, Kaneko discloses that the texture map comprises a set of mipmaps, further wherein the location field includes a plurality of subfields, each subfield identifying the location of one mipmap in the set of mipmaps. (See Abstract, Fig 1, Fig 2, col 2 line 35-col 4 line 39, col 5 line 8-32, col 6 line 6-56, col 11 line 27-55, col 11 line 57+)

Regarding claim 37, Kaneko discloses that the texture map spans a plurality of addresses in the memory device, the location field identifying the plurality of addresses. (See Abstract, Fig 1, Fig 2, col 2 line 35-col 4 line 39, col 5 line 8-32, col 6 line 6-56, col 11 line 27-55, col 11 line 57+)

Regarding claim 38, Kaneko discloses that the data structure is stored in the memory device, the memory device being texture memory. (See Abstract, Fig 1, Fig 2,

col 2 line 35-col 4 line 39, col 5 line 8-32, col 6 line 6-56, col 11 line 27-55, col 11 line 57+)

Claims 26-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaneko and Tanaka et al in view of Priem et al, and further in view of Chimoto (5,550,961).

Regarding claim 26, Kaneko discloses that the claimed feature of a method of storing a texture map in linear texture memory of a graphics accelerator, (See Abstract, Fig 1, Fig 2, col 2 line 35-col 4 line 39, col 5 line 8-32, col 6 line 6-56, col 11 line 27-55, col 11 line 57+) the method comprising:

a) determining the dimension of the texture map (See Abstract, Fig 1, Fig 2, col 2 line 35-col 4 line 39, col 5 line 8-32)

b) converting the texture map to a one dimensional texture map if the dimension of the texture map is determined to be more than one dimensional, the one dimensional texture map having a first number of consecutive data blocks (See Abstract, Fig 1, Fig 2, col 2 line 35-col 4 line 39, col 5 line 8-32)

c) locating a second number of consecutive memory locations in the texture memory, the first number being equal to the second number (See Abstract, Fig 1, Fig 2, col 2 line 35-col 4 line 39, col 5 line 8-32)

d) storing the one dimensional texture map in the located memory locations in the texture memory. (See Abstract, Fig 1, Fig 2, col 2 line 35-col 4 line 39, col 5 line 8-32)

Kaneko does not specifically disclose that texture data is relating to the dimensional type of its texture map. However, Priem et al discloses that the step of determine the change of dimensions in the texture map with respect to the change in the dimensions of pixel in the process of texture mapping. (See col 8 line 5-9, col 8 line 20-28) The motivation would have been to provide for much faster manipulation of the texture coordinates to obtain texture values and thereby eliminates the need for complicated and expensive circuitry in the graphics accelerator, as mentioned in the teaching of Priem et al. (See col 8 line 20-26) Therefore, it would have been obvious to one skilled in the art to incorporate the teaching of Priem et al into the teaching of Kaneko. Furthermore, the step of sorting the texture data with respect to the type of its dimension was well-know art to one having the ordinary skilled in the art, in order to operate texture mapping processing efficiently. The ordinary skilled in the art would know that the three-dimensional texture mapping process will require large capacity processor and much more time to process comparing to one-dimensional texture mapping process, since 3-D texture mapping have more variable to calculate. Therefore, it would have been obvious to one skilled in the art to separate the texture data by its dimensional type.

Also, the combination of Kaneko, Tanaka, Priem do not explicitly disclose that converting the multi-dimensional texture map into a one dimensional texture map. However, Chimoto discloses the way of express the two-dimensional texture data as one-dimensional texture data. (See Fig 3, col 2 line 50-55, col 5 line 12-39, col 6 line 67-col 7 line 39, col 7 line 55+) The motivation would have been to operate texturing, without extensive using of texture memory. Therefore, it would have been obvious to one skilled in the art to incorporate the teaching of Chimoto into the teaching of Kaneko.

Regarding claim 27, refer to the discussion for the claim 26 hereinabove, Chimoto discloses that step b) comprising:

B1) defining a plurality of data blocks within the texture map (See Fig 3, col 2 line 50-55, col 5 line 12-39, col 6 line 67-col 7 line 39, col 7 line 55+)

B2) assigning a sequence number to each of the data blocks, the sequence numbers being consecutive numbers. (See Fig 3, col 2 line 50-55, col 5 line 12-39, col 6 line 67-col 7 line 39, col 7 line 55+)

Regarding claim 28, refer to the discussion for the claim 26 hereinabove, Chimoto discloses that step d) comprising:

D1) consecutively storing each consecutive data block of the one dimensional texture map in the located memory locations. (See Fig 3, col 2 line 50-55, col 5 line 12-39, col 6 line 67-col 7 line 39, col 7 line 55+)

Regarding claims 29-31, claims 29-31 are similar in scope to the claims 26-28, and thus the rejections to claims 26-28 hereinabove are also applicable to claims 29-31.

Regarding claims 32-34, claims 32-34 are similar in scope to the claims 26-28, and thus the rejections to claims 26-28 hereinabove are also applicable to claims 32-34.

### ***Response to Arguments***

Applicant's arguments with respect to claims 1-38 have been considered but are moot in view of the new ground(s) of rejection.

### ***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks  
Washington, D.C. 20231

or faxed to:

(703) 308-9051, (for formal communications intended for entry)

Or:

(703) 308-6606 (for informal or draft communications, please label "PROPOSED" or "DRAFT").



Hand-delivered responses should be brought to Crystal Park II, 2021 Crystal Drive, Arlington, VA., Sixth Floor (Receptionist).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel J. Chung whose telephone number is (703) 306-3419. He can normally be reached Monday-Thursday and alternate Fridays from 7:30am - 5:00pm. If attempts to reach the examiner are unsuccessful, the examiner's supervisor, Michael, Razavi can be reached on (703) 305-4713. Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-4700.

djc  
September 21, 2001

A handwritten signature in black ink, appearing to read 'Matthew Luu', with a stylized flourish at the end.

**MATTHEW LUU**  
**PRIMARY EXAMINER**